NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
µPD3732

1760-BIT CCD LINEAR IMAGE SENSOR WITH PERIPHERAL CIRCUIT

The µPD3732 is a 1760-bit high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The µPD3732 has an output amplifier which has high gain and wide output range.

Built-in sample and hold circuit convert and output independent signal from CCD register in every bit to continuous video signal. So it is easy to interface to A/D converter or Bi-level converter.

FEATURES

- Valid photocell   1760-bit
- Photocell's pitch   14 µm
- High response sensitivity   Providing a response eight times better than the existing equivalent NEC product (µPD35H73) to the light from a daylight fluorescent lamp
- Peak response wavelength   550 nm (green)
- Resolution   8 dot/mm across the shorter side of an A4-size (210 x 297 mm) sheet
- Power supply   +12 V
- Drive clock level   CMOS output under 5 V operation
- High speed scan   0.9 ms/line
- Built-in circuit   Sample and hold circuit
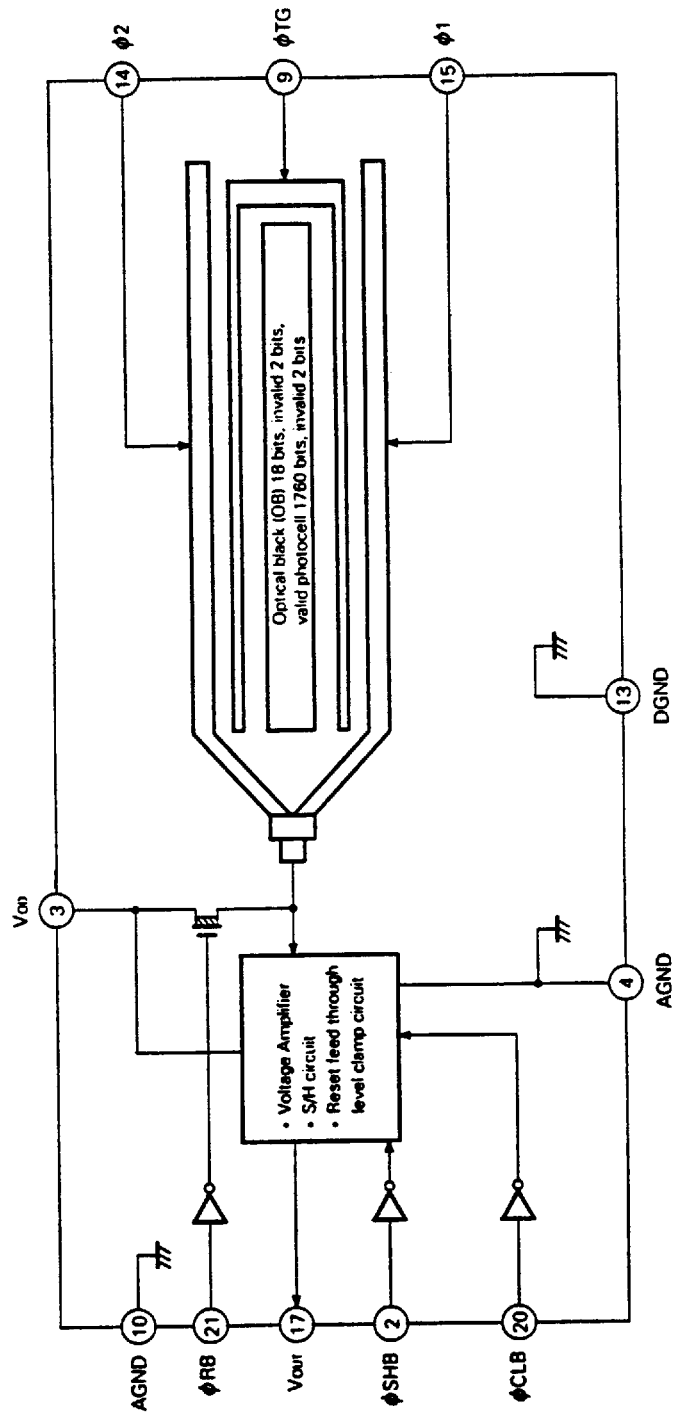 Reset feed through level clamp circuit

ORDERING INFORMATION

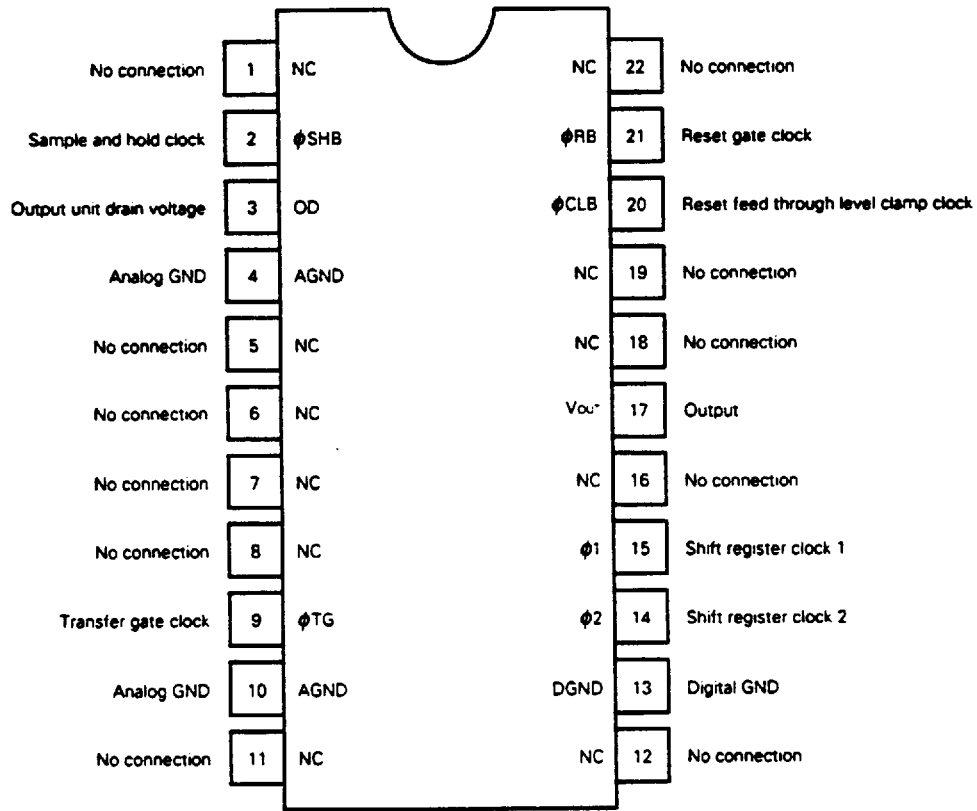| Part Number	Package	Quality Grade
µPD3732D	22-pin ceramic DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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BLOCK DIAGRAM

PIN CONFIGURATION (Top View)

No connection	1	NC	NC	22	No connection
Sample and hold clock	2	φSHB	φRB	21	Reset gate clock
Output unit drain voltage	3	OD	φCLB	20	Reset feed through level clamp clock
Analog GND	4	AGND	NC	19	No connection
No connection	5	NC	NC	18	No connection
No connection	6	NC	Vout	17	Output
No connection	7	NC	NC	16	No connection
No connection	8	NC	φ1	15	Shift register clock 1
Transfer gate clock	9	φTG	φ2	14	Shift register clock 2
Analog GND	10	AGND	DGND	13	Digital GND
No connection	11	NC	NC	12	No connection

PHOTOCELL STRUCTURE DIAGRAM

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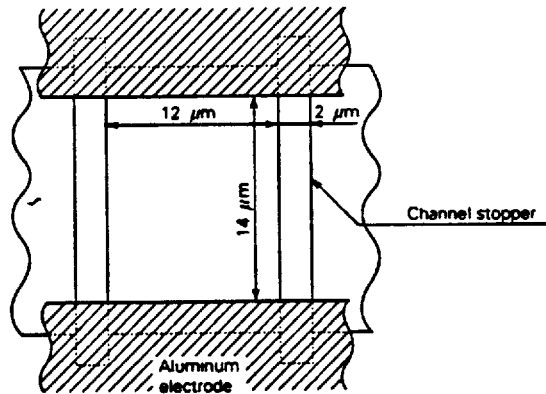
ABSOLUTE MAXIMUM RATINGS (T$_a$ = +25 ° C)

Parameter	Symbol	Ratings	Unit
Output unit drain voltage	V$_{OO}$	–0.3 to +15	V
Shift register clock voltage	V$_{\phi1, \phi2}$	–0.3 to +15	V
Reset signal voltage	V$_{\phi RB}$	–0.3 to +15	V
Transfer gate signal voltage	V$_{\phi TG}$	–0.3 to +15	V
Sample and hold signal voltage	V$_{\phi SH}$	–0.3 to +15	V
Reset feed through level clamp signal voltage	V$_{\phi CLB}$	–0.3 to +15	V
Operating ambient temperature	T$_{OPT}$	–25 to +60	°C
Storage temperature	T$_{STG}$	–40 to +100	°C

RECOMMENDED OPERATING CONDITIONS (T$_a$ = –25 to + 60 ° C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output unit drain voltage	V$_{OO}$	11.4	12.0	12.6	V
Shift register clock φ1, φ2 signal high level	V$_{\phi1H, \phi2H}$	4.5 (V$_{OO}$ –3)	5.0 (V$_{OO}$)	5.5 (V$_{OO}$ +0.6)	V
Shift register clock φ1, φ2 signal low level	V$_{\phi1L, \phi2L}$	–0.3 (–0.3)	0 (0)	0.5 (0.8)	V
Reset signal φRB high level	V$_{\phi RBH}$	4.5	5.0	5.5	V
Reset signal φRB low level	V$_{\phi RBL}$	–0.3	0	0.5	V
Transfer gate signal high level	V$_{\phi TGH}$	4.5 (V$_{OO}$ –3)	5.0 (V$_{OO}$)	5.5 (V$_{OO}$ +0.6)	V
Transfer gate signal low level	V$_{\phi TGL}$	–0.3 (–0.3)	0 (0)	0.5 (0.8)	V
Sample and hold signal high level	V$_{\phi SHH}$	4.5	5.0	5.5	V
Sample and hold signal low level	V$_{\phi SHL}$	–0.3	0	0.5	V
Reset feed through level clamp signal high level	V$_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed through level clamp signal low level	V$_{\phi CLBL}$	–0.3	0	0.5	V
Data rate	f$_{\phi n}$	0.2	1	2	MHz

Remark Values in ( ) are for the driver under 12 V operation.

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ELECTRICAL CHARACTERISTICS

$\left(\begin{array}{l} T_a = +25\,°C,\ V_{DD} = 12\ V,\ f_{\phi 1} = 0.5\ MHz,\ data\ rate = 1\ MHz,\ storage\ time = 10\ ms \\ light\ source:\ 3200\ K\ halogen\ lamp + C500\ (infrared\ cut\ filter),\ input\ clock = 5\ V_{P-P} \end{array} \right)$

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{SAT}		1.5	2.0		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.022		lx·s
Photo response non-uniformity	PRNU	$V_{OUT} = 500$ mV		±2	±8	%
Average dark signal	ADS	Light shielding		1.0	8.0	mV
Dark signal non-uniformity	DSNU	Light shielding	−8	±4	+8	mV
Power consumption	P_W			140	180	mW
Output impedance	Z_O			0.5	1	kΩ
Response	R_F	Daylight color fluorescent lamp	63	90	117	V/lx·s
	R_W	W lamp		270		
Response peak wavelength				550		nm
Image lag	IL	$V_{OUT} = 1$ V		7		%
Offset level (Note 1)	V_{OS}	When ϕCLB is input	3.5	4.5	5.5	V
Input capacitance of shift register clock pin	$C_{\phi 1}$ $C_{\phi 2}$			400		pF
Input capacitance of reset pin	$C_{\phi RS}$			5		pF
Input capacitance of sample and hold pin	$C_{\phi SH}$			5		pF
Input capacitance of reset feed through level pin	$C_{\phi CLB}$			5		pF
Input capacitance of transfer gate signal pin	$C_{\phi TG}$			100		pF
Output rise delay time	t_O			120		ns
Register imbalance	RI	$V_{OUT} = 500$ mV			3	%
Transfer efficiency	TTE	$V_{OUT} = 1$ V, data rate = 2 MHz	92			%
Dynamic range	DR	V_{SAT}/DSNU		500		times
Reset feed through noise	RFSN		0	1000	1800	mV
Sample and hold noise	SHSN		−50	0	50	mV
Bit noise 1	BN1	When ϕCLB is input		4		mV_{P-P}
Bit noise 2 (Note 2)	BN2	When ϕCLB is not input (in case of inputting ϕRB clock signal to ϕCLB pin)		16		mV_{P-P}
Resolution	MTF	Modulation transfer function at nyquist frequency		65		%

Note 1. In case of inputting ϕRB clock signal to ϕCLB pin, offset level decreases corresponding to RFSN.

2. When ϕCLB is not used (in case of inputting ϕRB clock signal to ϕCLB pin), because of 1/f noise of output amplifier, compared with bit noise 1 (BN1), bit noise increases.

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TIMING CHART 1
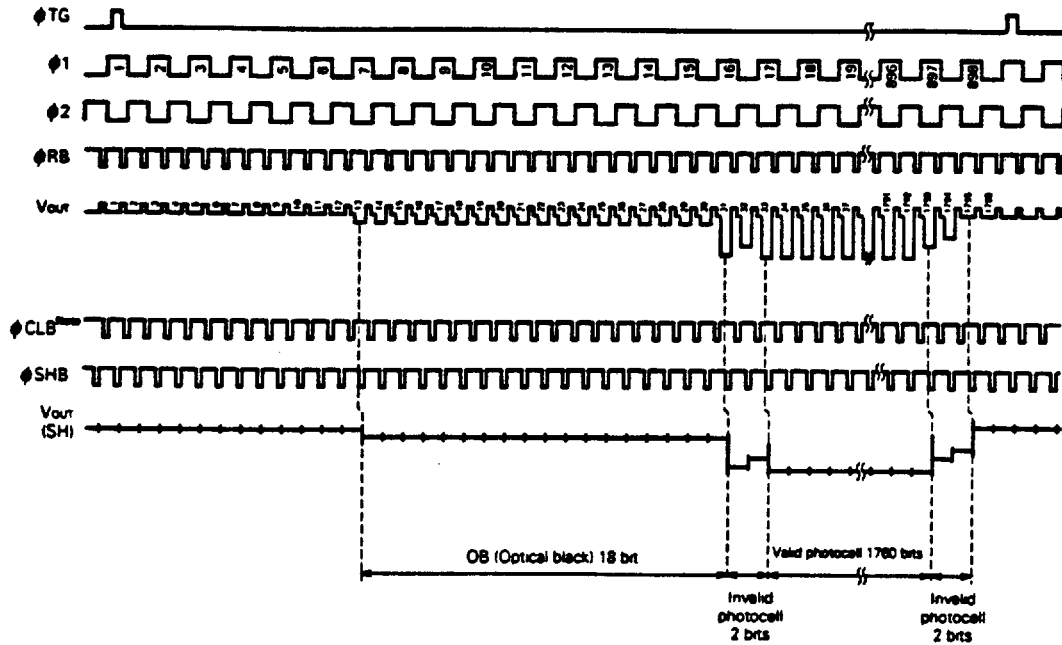
Remark Vᴏᴜᴛ = Output when φSHB is not used (When φSHB is not used, connect φSHB pin to GND)

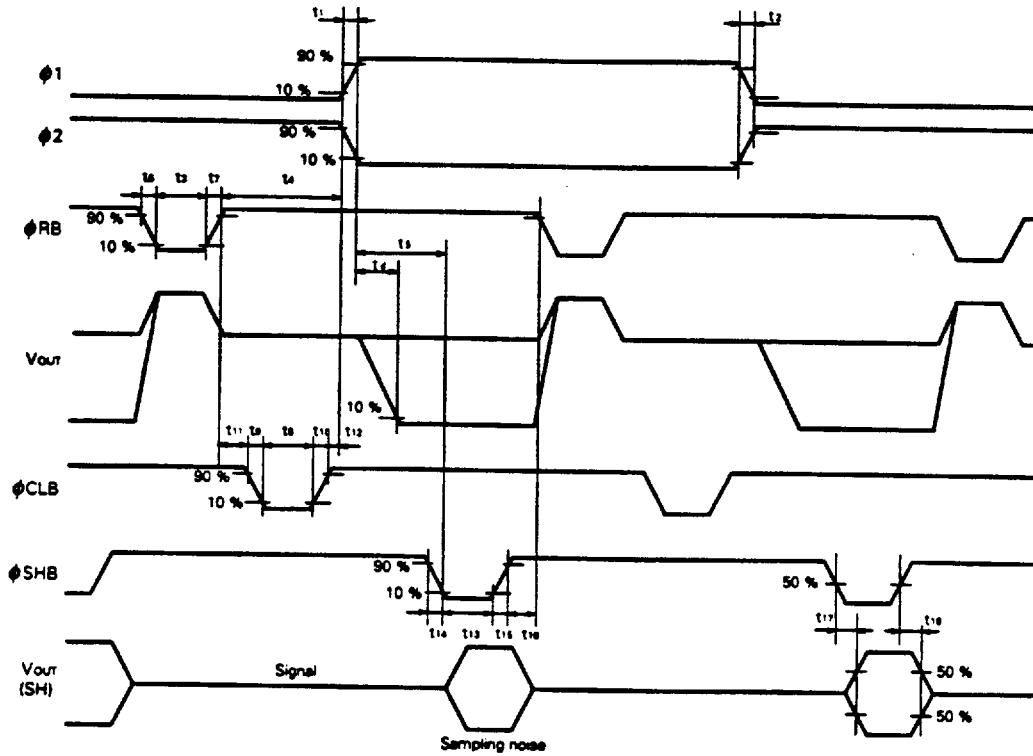Vᴏᴜᴛ (SH) = Output when φSHB is used.

When φCLB is used, reset feed through level of Vᴏᴜᴛ is clamped to a certain level.

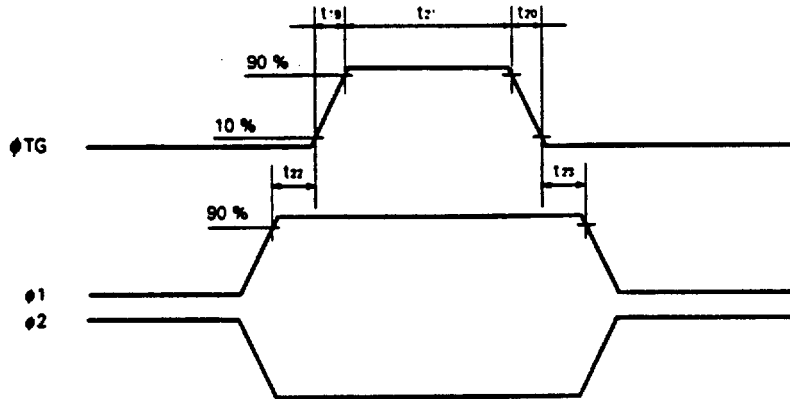(When φCLB is not used, input φRB clock to φCLB pin)

Note When φCLB is not used (in case of inputting φRB clock signal to φCLB pin), because of 1/f noise of output amplifier, bit noise increases. Therefore use φCLB.
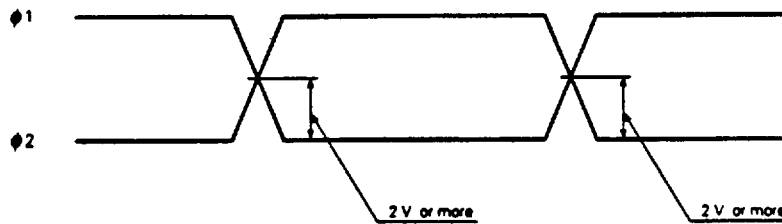
TIMING CHART 2

Remark Vout (SH) = Output when φSHB is used.

TIMING CHART for ϕTG, ϕ1, ϕ2

CROSS POINTS for ϕ1, ϕ2

Remark Adjust cross point of ϕ1, ϕ2 by ϕ1, ϕ2 pin input resistors.

(Unit: ns)

Parameter	MIN.	TYP.	MAX.
t_1, t_2	0	50	(100)
t_3	20	100	–
t_4 (Note)	220	300	–
t_5	150	300	–
t_6, t_7	0	50	–
t_8	20	100	–
t_9, t_{10}	0	50	–
t_{11}	150	250	–
t_{12}	20	50	–
t_{13}	80	100	–
t_{14}, t_{15}, t_{16}	0	50	–
t_{17}	0		
t_{18}		5	10
t_{19}, t_{20}	0	50	–
t_{21}	650	1000	(2000)
t_{22}, t_{23}	0	100	–

Note When ϕCLB is not used (in case of inputting ϕRB clock signal to ϕCLB pin), t_4 = 20 ns MIN.

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD3732 is destroyed.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. **Saturation voltage: V_{SAT}**
   Output signal voltage at which the response linearity is lost.

2. **Saturation exposure: SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. **Photo response non-uniformity: PRNU**
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU\ (\%) = \left(\frac{V_{MAX.}\ or\ V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n}V_i} - 1 \right) \times 100$$

   n : Number of valid bits
   V_i : Output voltage of each bit
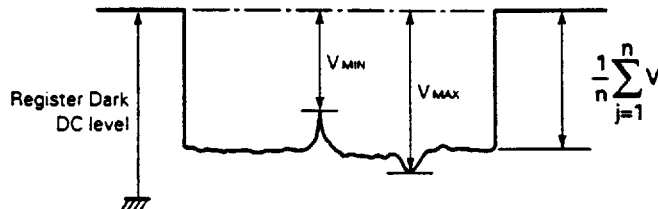
4. **Average dark signal: ADS**
   Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n}V_i$$

5. **Dark signal non-uniformity: DSNU**
   The difference between peak or bottom output voltage in light shielding and ADS.
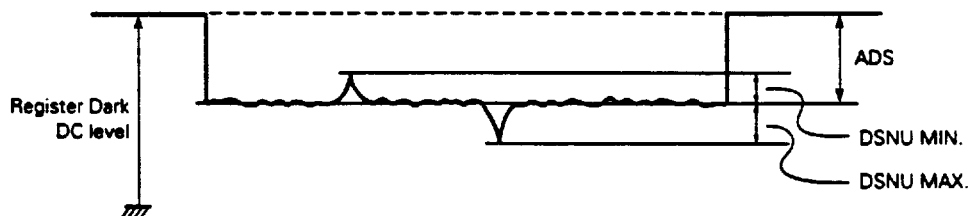
6. **Output impedance: Z_o**
   Output pin impedance viewed from outside.

7. **Response: R**
   Output voltage divided by exposure (lx·s).
   Note that the response varies with the light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.

$$Lag = \frac{V_1}{V_{OUT}} \times 100 \ (\%)$$
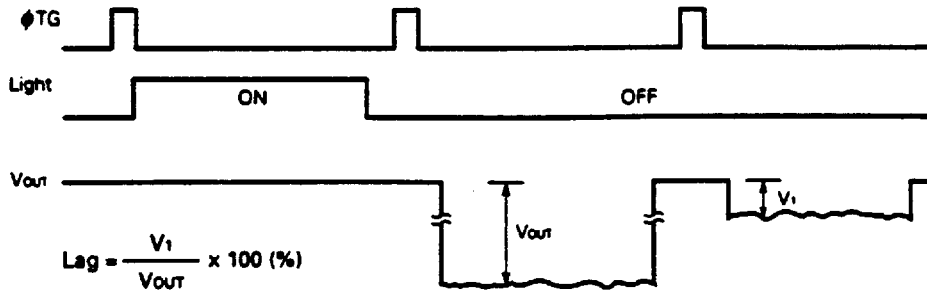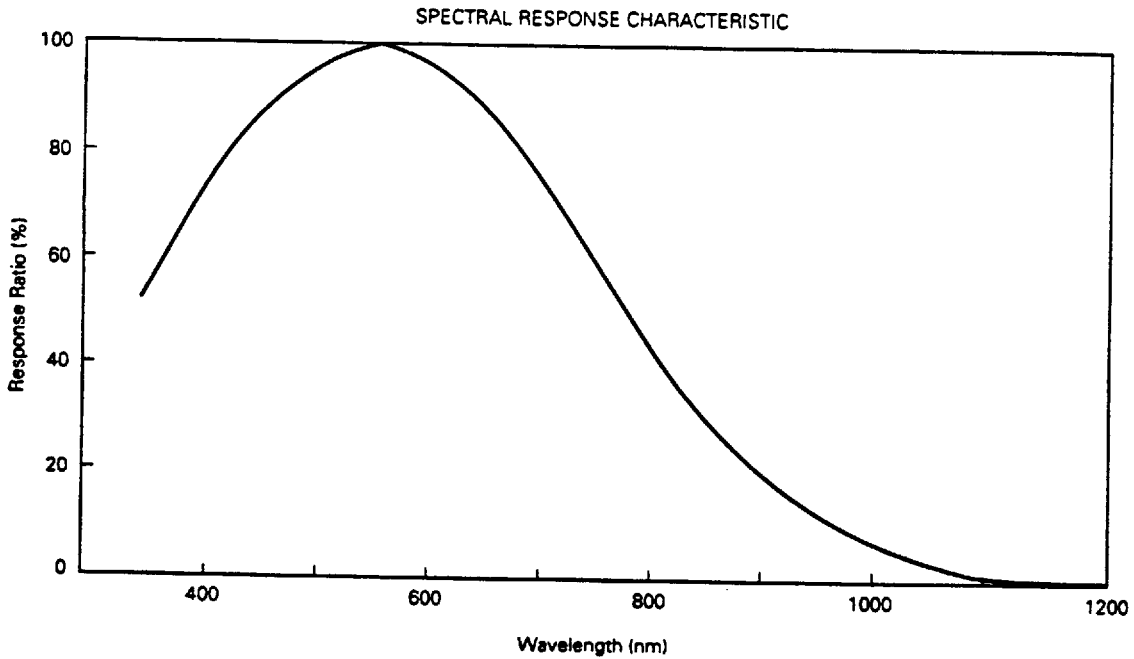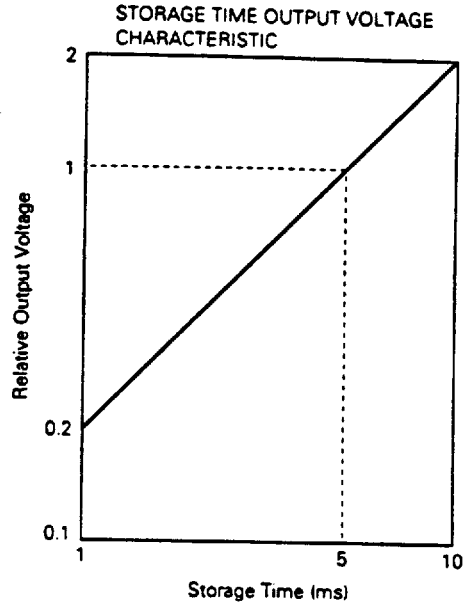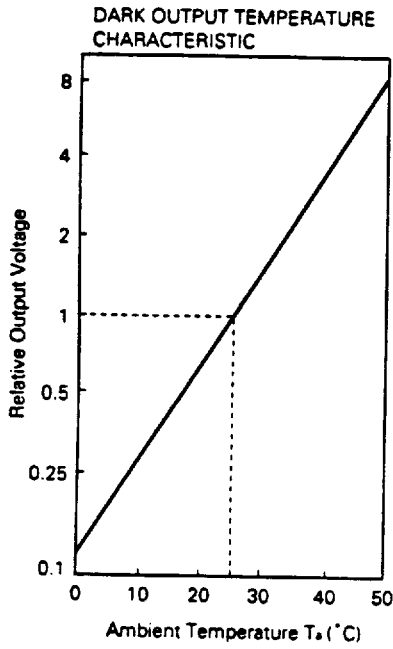
9. Register Imbalance: RI

The rate of the average voltage which is the difference between the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

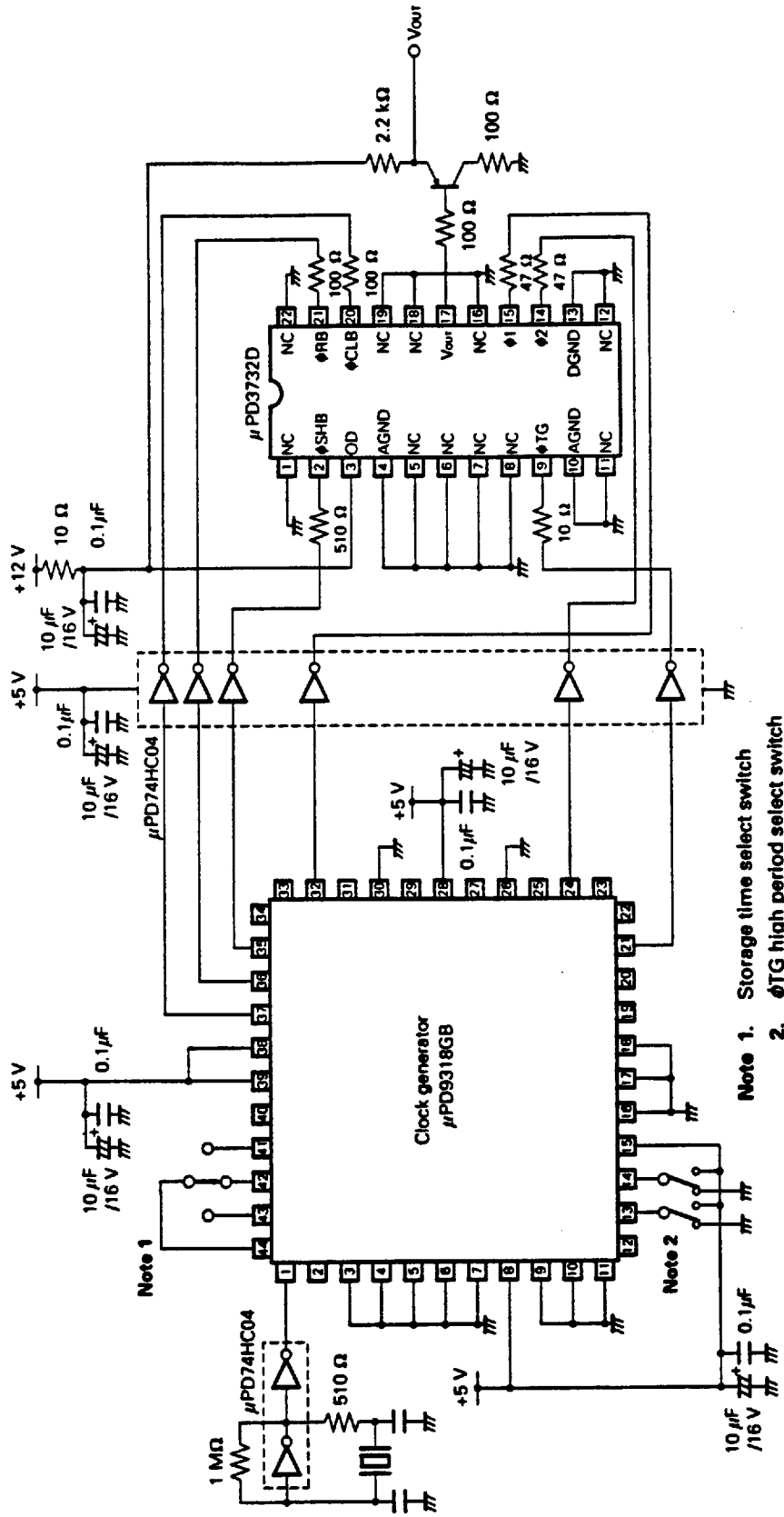$$RI = \frac{\frac{1}{n}\sum_{j=1}^{n} |V_i - V_{i+1}|}{\frac{1}{n}\sum_{j=1}^{n} V_i} \times 100 \ (\%)$$

10. Bit Noise: BN

Output signal distribution of a photocell by scan.

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STANDARD CHARACTERISTIC CURVES (T$_a$ = +25 ° C)

DARK OUTPUT TEMPERATURE
CHARACTERISTIC

STORAGE TIME OUTPUT VOLTAGE
CHARACTERISTIC

SPECTRAL RESPONSE CHARACTERISTIC

**APPLICATION EXAMPLE**

Note 1. When internal sample and hold circuit of μPD3732 is not used, connect pin 2 (φSHB) to GND.
   2. When internal reset feed through level clamp circuit of μPD3732 is not used, input φRB clock signal to pin 20 (φCLB).
   3. When φCLB is not used (in case of inputting φRB clock signal to φCLB pin), because of 1/f noise of output amplifier, bit noise increases.

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

Remark 1. Storage time select switch
   2. φTG high period select switch

PACKAGE DIMENSIONS (Unit: mm)
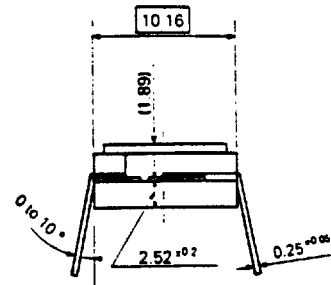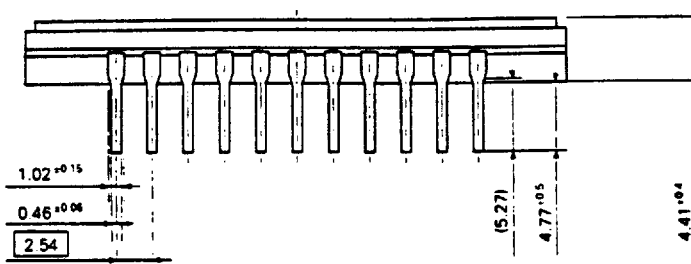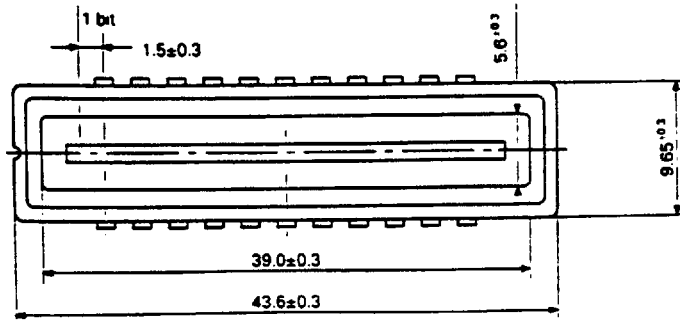
Name	Dimensions	Refractive index
Glass cap	42.2 x 9.0 x 0.5	1.5